AMENDMENT

Please amend the claims as follows:

Please cancel claims 44-83.

Please add new claims 84 - 178

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84. (new) A memory element, comprising:

a first dielectric layer;

a electrical contact formed on said first dielectric layer;

a second dielectric layer formed on said electrical contact, said electrical contact having an edge between said first and second dielectric layers; and

a programmable resistance material in electrical communication with said electrical contact, substantially all of said electrical communication occurring through at least a portion of said edge.

85. (new) The memory element of claim 84, wherein said edge is adjacent to said programmable resistance material.

86. (new) The memory element of claim 84, wherein said edge includes one or more protruding portions, substantially all of said communication occurring through at least one of said protruding portions.

87. (new) The memory element of claim 84, wherein said edge includes one or more protruding portions extending to terminal ends adjacent said programmable resistance material, substantially all of said electrical communication occurring through said terminal ends.

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88. (new) The memory element of claim 84, wherein said electrical contact comprises a conductive layer.

89. (new) The memory element of claim 84, wherein said electrical contact comprises a plurality of conductive layers.

90. (new) The memory element of claim 84, wherein said electrical contact comprises at least a first conductive layer formed on said first dielectric layer and a second conductive layer formed on said first conductive layer.

91. (new) The memory element of claim 90, wherein the resistivity of the first conductive layer is less than the resistivity of said second conductive layer.

92. (new) The memory element of claim 84, wherein said first dielectric layer has a sidewall surface, said electrical contact being formed on said sidewall surface.

93. (new) The memory element of claim 92, wherein said edge includes one or more protruding portions, substantially all of said electrical communication occurring through at least one of said protruding portions.

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94. (new) The memory element of claim 92, wherein said edge includes one or more protruding portions extending to terminal ends adjacent said programmable resistance material, substantially all of said electrical communication occurring through said terminal ends.

95. (new) The memory element of claim 92, wherein said electrical contact comprises a conductive layer formed on said sidewall surface.

96. (new) The memory element of claim 92, wherein electrical contact includes at least a first conductive layer formed on said sidewall surface and a second conductive layer formed on first conductive layer.

97. (new) The memory element of claim 96, wherein the resistivity of said first conductive layer is less than the resistivity of said second conductive layer.

B1 98. (new) The memory element of claim 96, wherein substantially all electrical communication between said electrical contact and said programmable resistance material is through at least a portion of an edge of said second conductive layer.

99. (new) The memory element of claim 96, wherein said first conductive layer comprises at least one material selected from the group consisting of titanium tungsten, tungsten silicide, tungsten, molydenum, N+ doped polysilicon and titanium nitride.

100. (new) The memory element of claim 96, wherein said second conductive layer comprises at least one material selected from the group consisting of titanium nitride,

titanium carbonitride, titanium aluminum nitride, titanium silicon nitride, carbon, and N- doped polysilicon.

101. (new) The memory element of claim 92, wherein said electrical contact is a sidewall layer formed on said sidewall surface.

102. (new) The memory element of claim 92, wherein said electrical contact is a conductive sidewall spacer formed on said sidewall surface.

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103. (new) The memory element of claim 102, wherein said sidewall spacer comprises one or more conductive layers.

104. (new) The memory element of claim 103, wherein said conductive sidewall spacer comprises at least a first sidewall layer formed on said sidewall surface of said first dielectric layer and a second sidewall layer formed on said first sidewall layer.

105. (new) The memory element of claim 104, wherein the resistivity of said first sidewall layer is less than the resistivity of said second sidewall layer.

106. (new) The memory element of claim 104, wherein said first sidewall layer comprises at least one material selected from the group consisting of titanium tungsten, tungsten silicide, tungsten, molydenum, N+ doped polysilicon and titanium nitride.

107. (new) The memory element of claim 104, wherein said second sidewall layer comprises at least one material selected from the group consisting of titanium nitride, titanium carbonitride, titanium aluminum nitride, titanium silicon nitride, carbon, and N- doped polysilicon.

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108. (new) The memory element of claim 104, wherein substantially all of said electrical communication between said electrical contact and said programmable resistance material occurs through an edge of said second sidewall layer.

109. (new) The memory element of claim 102, wherein said conductive spacer is substantially flat.

110. (new) The memory element of claim 102, wherein said conductive spacer is cylindrical or tubular.

111. (new) The memory element of claim 92, wherein said electrical contact is a conductive liner, a portion of said conductive liner being formed on said sidewall surface.

112. (new) The memory element of claim 108, wherein said conductive liner is cup-shaped.

113. (new) The memory element of claim 92, wherein said electrical contact is a cup-shaped electrical contact having an open end adjacent said programmable resistance material.

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114. (new) The memory element of claim 92, wherein said sidewall surface defines an opening in said first dielectric layer, said electrical contact formed on the sidewall surface of said opening.

115. (new) The memory element of claim 113, wherein said opening is a trench or a via hole.

116. (new) The memory element of claim 114, wherein said via hole is substantially round.

117. (new) The memory element of claim 114, wherein said opening passes through said first dielectric layer and exposes an underlying substrate.

118. (new) The memory element of claim 113, wherein said opening has a bottom surface, said electrical contact being formed on a first portion of the bottom surface of said opening and said second dielectric layer is formed on a second portion of the bottom surface of said opening.

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119. (new) The memory element of claim 113, wherein said electrical contact is formed on substantially the entire bottom surface of said opening.

120. (new) The memory element of claim 92, wherein said sidewall surface is a sidewall surface of a raised portion of said first dielectric layer.

121. (new) The memory element of claim 84, wherein said electrical contact is a substantially vertically disposed conductive layer.

122. (new) The memory element of claim 84, wherein said electrical contact is substantially horizontally disposed conductive layer.

123. (new) The memory element of claim 84, wherein said edge is adjacent to a sidewall surface of said programmable resistance material.

124. (new) The memory element of claim 84, wherein said edge at least partially circumscribes said programmable resistance material.

125. (new) The memory element of claim 84, wherein said edge forms a band at least partially around said programmable resistance material.

126. (new) The memory element of claim 84, wherein said electrical contact has a thickness between 50 and 1000 Angstroms at the area of contact with said memory material.

127. (new) The memory element of claim 84, wherein the area of contact between said programmable resistance material and said electrical contact is at least a portion of an annulus.

128. (new) The memory element of claim 84, wherein said electrical contact comprises at least one material selected from the group consisting of titanium nitride, titanium aluminum nitride, titanium carbonitride, titanium silicon nitride, carbon, N- doped polysilicon, titanium tungsten, tungsten silicide, tungsten, molydenum, N+ doped polysilicon.

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129. (new) The memory element of claim 84, wherein said programmable resistance material includes a phase change material.

130. (new) The memory element of claim 84, wherein said programmable resistance material includes a chalcogen element.

131. (new) A memory element, comprising:

a first dielectric layer having a sidewall surface;

a conductive layer formed on said sidewall surface;

a second dielectric layer formed on said conductive layer, said conductive layer having an edge between said first and second dielectric layers;

and

a programmable resistance material in electrical communication with said conductive layer, substantially all of said electrical communication occurring through at least a portion of said edge.

132. (new) The memory element of claim 130, wherein said edge is adjacent to said programmable resistance material.

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133. (new) The memory element of claim 132, wherein substantially all of the remainder of said conductive layer is remote to said programmable resistance material.

134. (new) The memory element of claim 131, wherein said edge is the top edge of said conductive layer.

135. (new) The memory element of claim 131, wherein said edge includes one or more protruding portions, substantially all of said communication occurring through at least one of said protruding portions.

136. (new) The memory element of claim 131, wherein said edge includes one or more protruding portions extending to terminal ends adjacent said programmable resistance

material, substantially all of said electrical communication occurring through said terminal ends.

137. (new) The memory element of claim 131, wherein said conductive layer is a sidewall layer formed on said sidewall surface.

138. (new) The memory element of claim 131, wherein said conductive layer is a conductive sidewall spacer formed on said sidewall surface.

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139. (new) The memory element of claim 131, wherein said conductive layer is a conductive liner, a portion of said conductive liner being formed on said sidewall surface.

140. (new) The memory element of claim 131, wherein said sidewall surface defines an opening in said first dielectric layer, said conductive layer being formed on the sidewall surface of said opening.

141. (new) The memory element of claim 140, wherein said opening is a trench or a via hole.

142. (new) The memory element of claim 142, wherein said opening has a bottom surface, said conductive layer being formed on a first portion of a bottom surface of said opening and said second dielectric layer is formed on a second portion of the bottom surface of said opening.

143. (new) The memory element of claim 142, wherein said conductive layer is formed on substantially the entire bottom surface of said opening.

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144. (new) The memory element of claim 131, wherein said sidewall surface is the sidewall surface of a raised portion of said first dielectric layer.

145. (new) The memory element of claim 131, wherein said raised portion of said first dielectric layer is a pillar or a mesa.

146. (new) The memory element of claim 131, wherein said conductive layer has a thickness between 50 and 1000 Angstroms at the area of contact with said programmable resistance material.

147. (new) The memory element of claim 131, wherein said conductive layer comprises at least one material selected from the group consisting of titanium nitride, titanium aluminum nitride, titanium carbonitride, titanium silicon nitride, carbon, N- doped polysilicon, titanium tungsten, tungsten silicide, tungsten, molydenum, and N+ doped polysilicon.

148. (new) The memory element of claim 131, wherein said programmable resistance material includes a phase change material.

149. (new) The memory element of claim 131, wherein said programmable resistance material includes a chalcogen element.

150. (new) A memory element, comprising:

a programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material, said electrical contact formed on a sidewall surface of a dielectric layer, said electrical contact extending on said sidewall surface to an edge adjacent said programmable resistance material, substantially all of said electrical communication

occurring through at least a portion of said edge of said electrical contact.

151. (new) The memory element of claim 150, wherein said electrical contact has a thickness between 50 and 1000 Angstroms at the area of contact with said programmable resistance material.

152. The memory element of claim 150, wherein said electrical contact is a conductive layer.

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153. (new) The memory element of claim 150, wherein said electrical contact is a conductive sidewall spacer.

154. (new) The memory element of claim 150, wherein said electrical contact is a conductive sidewall liner.

155. (new) The memory element of claim 150, wherein said electrical contact includes at least a first conductive layer formed on said dielectric layer and a second conductive layer formed on said first conductive layer.

156. (new) The memory element of claim 150, wherein said electrical contact is cup-shaped.

157. (new) The memory element of claim 153, wherein said conductive spacer comprises at least first conductive sidewall layer formed on said sidewall surface and a second conductive sidewall layer formed on said first conductive sidewall layer.

158. (new) The memory element of claim 157, wherein the resistivity of said first sidewall layer is less than the resistivity of said second sidewall layer.

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159. (new) The memory element of claim 153, wherein substantially all of said communication between said electrical contact and said programmable resistance material occurs through at least a portion of an edge of said second sidewall layer.

160. (new) The memory element of claim 150, wherein said edge includes one or more protruding portions, substantially all of said electrical communication occurring through at least one of said protruding portions.

161. (new) The memory element of claim 150, wherein said edge includes one or more protruding portion extending to terminal ends adjacent to said programmable resistance

material, substantially all of said electrical communication occurring through said terminal ends.

162. (new) The memory element of claim 150, wherein said sidewall surface defines an opening in said dielectric layer.

163. (new) The memory element of claim 150, wherein said electrical contact comprises at least one material selected from the group consisting of titanium nitride, titanium aluminum nitride, titanium carbonitride, titanium silicon nitride, carbon, N- doped polysilicon, titanium tungsten, tungsten silicide, tungsten, molydenum, and N+ doped polysilicon.

164. (new) The memory element of claim 150, wherein said programmable resistance material comprises a phase change material.

165. (new) The memory element of claim 150, wherein said programmable resistance material comprises a chalcogen element.

166. (new) A memory element, comprising:

a programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material, said electrical contact formed on a sidewall surface of a dielectric layer, said electrical contact extending on said sidewall surface to a terminal portion adjacent said memory material, said terminal portion having a thickness between 50 and 1000 Angstroms, substantially all of said electrical communication occurring through said terminal portion.

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167. (new) The memory element of claim 166, wherein said terminal portion has a thickness between 50 and 500 Angstroms.

168. (new) The memory element of claim 166, wherein said electrical contact comprises at least one conductive layer.

169. (new) The memory element of claim 166, wherein said electrical contact is a conductive spacer.

170. (new) The memory element of claim 166, wherein said electrical contact is a conductive liner.

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172. (new) The memory element of claim 166, wherein said electrical contact is cup-shaped.

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173. (new) The memory element of claim 166, wherein said sidewall surface defines an opening in said dielectric layer.

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174. (new) The memory element of claim 166 wherein the area of contact between said electrical contact and said programmable resistance material has a dimension between 50 and 1000 Angstroms in at least one direction.

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175. (new) The memory element of claim 166, wherein the area of contact between said electrical contact and said programmable resistance material has a dimension between 100 and 500 Angstroms in at least one direction.

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176. (new) The memory element of claim 166, wherein said electrical contact comprises at least one material selected from the group consisting of titanium nitride, titanium aluminum nitride, titanium carbonitride, titanium silicon nitride, carbon, N- doped polysilicon, titanium tungsten, tungsten silicide, tungsten, molydenum, N+ doped polysilicon.

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~~177~~. (new) The memory element of claim 166, wherein said programmable resistance material comprises a phase change material.

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B1 ~~178~~. (new) The memory element of claim 166, wherein said programmable resistance material comprises a chalcogen element.